

Remarks/Arguments:

Claims 1-18 are pending in the above-identified application. Claims 13-17/13 were withdrawn.

Claims 1, 17/1 and 18 were rejected under 35 U.S.C. § 102 (e) as being anticipated by Grewing et al. Claim 1 is amended to include,

... said n pieces of variable capacitance circuit including first, second and third variable capacitance circuits, ...

...a first reference voltage is inputted to one of the terminals of said first variable capacitance circuit, a second reference voltage is inputted to one of the terminals of said second variable capacitance circuit and a third reference voltage is inputted to one of the terminals of said third variable capacitance circuit and said first, second and third reference voltages are fixed and different from each other.

Basis for these amendments may be found in the specification at page 20, lines 14-25 and Figure 1. With regard to claim 1, Grewing et al. does not disclose or suggest three reference voltages inputted to associated variable capacitance circuits and that each of the three reference voltages are fixed and different from each other. The single figure in Grewing et al. includes a first reference voltage C and a second reference voltage 7. Grewing et al. does not include a third reference voltage inputted to a third variable capacitance circuit. The reference to Grewing et al., however, does not disclose three reference voltages inputted to associated variable capacitance circuits.

As shown in Figure 1 of the present application, the first reference voltage (V_{ref}) is inputted to the first variable capacitance circuit A. The second reference voltage ($V_{ref}-V_d$) is inputted to the second variable capacitance circuit B. The third

Application No.: 10/676,654
Amendment Dated: July 19, 2006
Reply to Office Action of: April 24, 2006

MTS-3475US

reference voltage ($V_{ref} - 2V_d$) is inputted to the third variable capacitance circuit C. Applicant's claimed feature of three reference voltages inputted to associated variable capacitance circuits and that each of the three reference voltages are fixed and different from each other is advantageous over the prior art because a total capacitance of the variable capacitance circuits slowly increases against the control voltage and a change in oscillation frequency may be rendered moderate over a wide range of the control voltage.

Because Grewing et al. does not disclose or suggest the features of claim 1, claim 1 is not subject to rejection under 35 U.S.C. § 102(e) in view of Grewing et al. Claim 17/1 depends from claim 1. Accordingly, claim 17/1 is not subject to rejection under 35 U.S.C. § 102(e) in view of Grewing et al.

With regard to claim 18, claim 18, while not identical to claim 1, includes features similar to those set forth above with regard to claim 1. Thus, claim 18 is also allowable over the art of record for reasons similar to those set forth above with regard to claim 1.

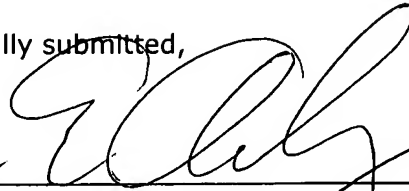
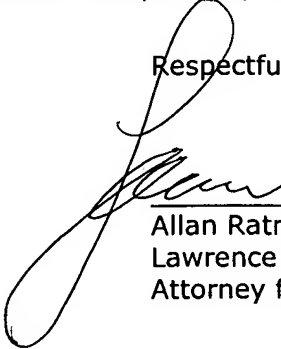
Claim 12 was rejected under 35 U.S.C. § 103 (a) as being anticipated by Grewing et al. and Friedman et al. Grewing et al. is described above. Friedman et al. is described in the previous response. Friedman et al. does not disclose or suggest Applicant's claimed feature of three reference voltages inputted to associated variable capacitance circuits and that each of the three reference voltages are fixed and different from each other. Neither Grewing et al., Friedman et al. nor their combination disclose or suggest the features of claim 1. Claim 12 depends from claim 1. Accordingly, claim 12 is not subject to rejection under 35 U.S.C. § 103 (a) in view of Grewing et al. and Friedman et al.

Application No.: 10/676,654
Amendment Dated: July 19, 2006
Reply to Office Action of: April 24, 2006

MTS-3475US

In view of the foregoing amendments and remarks, this Application is in condition for allowance which action is respectfully requested.

Respectfully submitted,



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Fran Petrillo

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